Design and Evaluation of Nonlinear MPC for Active Load Balancing in Adjacent Battery Cells ⋆

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Abstract: Active load balancing in battery cells has significant advantages in energy storage systems and electric vehicles (EVs). However, diversity in balancing network power electronics components, energy transfer paths, etc., leads to a multitude of architectures and topologies, each yielding varying performance, complexity, and cost. Therefore, this work implements and compares the load balancing performance of (i) series, (ii) module, and (iii) layer-based adjacent battery cell network topologies, each managed by a different nonlinear model predictive control (NMPC) strategy. The solution is built on the dynamics of active balancing networks and battery cells and incorporates high-fidelity balancing currents to characterize the load using state of charge (SOC). The simulation results, which are performed on twelve adjacent cells, reveal that load balancing in cells connected in layer-based topology is achieved in 1430 s. While series and module-based topologies achieved the load balancing objective in 2980 and 2770 s, respectively.

Keywords: Electric vehicle; model predictive control; applications of power electronics; constraint control system; decentralized control

1. INTRODUCTION

Forming the backbone of energy storage systems and electric vehicles (EVs), batteries have a critical role to play. Moreover, due to the limited voltage supply of a single cell, they are usually connected in a string of series and parallel configurations to meet the demands of high-end power applications (Qi et al. (2022)). However, this setting usually leads to a charge imbalance among cells that subsequently affects the battery's performance. Therefore, load balancing, which is broadly categorized as active (ALB) and passive balancing, can ameliorate these impacts. Moreover, based on balancing circuits, control schemes, interconnection of cells, and paths of energy transfer, the balancing strategies are further subcategorized into architectures and topologies. Thus this flexibility in design parameters leads to various balancing systems, with each suited for a specific application and yielding different performance, such as balancing time (BT), ease of implementation, computational time, etc. (Ma and Gao (2024)).

Lukasiewycz et al. (2016) provided an automated synthesis framework to formulate a balancing circuit and its control. Ouyang et al. (2024) proposed a hypergraph-based approach in an attempt to unify the modeling for ALB topologies. This scheme facilitated determining the minimum number of equalizers required for balancing, and by finding a correlation between BT and the graph's Laplacian matrix, they were able to streamline the process of evaluating various topologies. Khan et al. (2024) introduced an H-bridge into a duty cycle balancing (DCB) and cell-to-pack balancing scheme, forming H-DCB, to bypass certain cells in 96 serially connected cell configurations. Using simulation, the authors demonstrated the efficiency of the proposed scheme relative to conventional DCB, achieving 1.5 times faster balancing speed. To reduce the communication and processing overhead, Chatzinikolaou and Rogers (2017) introduced a hierarchical balancing strategy to perform cell balancing and other objectives. By using a decentralized battery management system and multiple control layers, the authors achieved balancing within 2 mV. Similarly, to reduce the architecture's complexity, Wei et al. (2021) employed a constant current strategy to balance the battery's voltages. By using LCC multiresonant as a common equalizer, the proposed work transferred charge from a string of cells to a single cell in an open loop setting. Bani Ahmad et al. (2022) proposed a topology that eliminated the need for balancing three branches of battery systems and reduced it to just a single branch. Their approach involved making use of idle cells, treating them as redundant units that can be dropped while balancing, subsequently leading to lower operational costs. Furthermore, Ghaeminezhad et al. (2021) provided a comparative performance of various topologies, such as

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adjacent, non-adjacent, and mixed topologies, in terms of equalization speed, hardware implementation, economic viability, etc.

In literature, various balancing architectures and topologies have been proposed. For instance, in our previous works Javed et al. (2022) and Javed et al. (2024a), we formulated high-fidelity modeling of four different architectures and performed balancing using a simple control scheme. Therein, we demonstrated that including the dynamic balancing parameters had a significant impact on ALB performance. Similarly, Uppal et al. (2023), and Azam et al. (2024) extended that by using nonlinear model predictive control (NMPC) on buck-boost (BB) architecture and integrating the thermal model, respectively. Therefore, this work aims to integrate the high-fidelity modeling currents into the NMPC framework to evaluate the performance in terms of BT and computational cost for three distinct balancing topologies: series-based cell-to-cell (SB), module-based (MB), and layer-based (LB) topologies.

The rest of the paper is organized as follows: Section 2 outlines the mathematical modeling of each topology, and NMPC problem is formulated for ALB in Section 3; the results are discussed in Section 4, and, finally, the paper is concluded in 5.

2. MATHEMATICAL MODELING

The mathematical models of SB, MB, and LB cell-cell active cell balancing topologies are presented in this section. The atomic unit for all the topologies that balances the SoC levels of two adjacent cells n and $n+1$ has been depicted in Fig. 1. For transferring charge amongst the cells, a bi-directional BB converter is employed, and the dynamics of a Li-ion cell is represented using a simplified equivalent circuit model (ECM)–an open circuit voltage source v_n and a resistor R_{0_n} in series representing the internal resistance of the cell n. The mathematical model of the atomic unit shown in Fig. 1 is given as follows:

2.1 Mathematical Model of the Atomic Unit

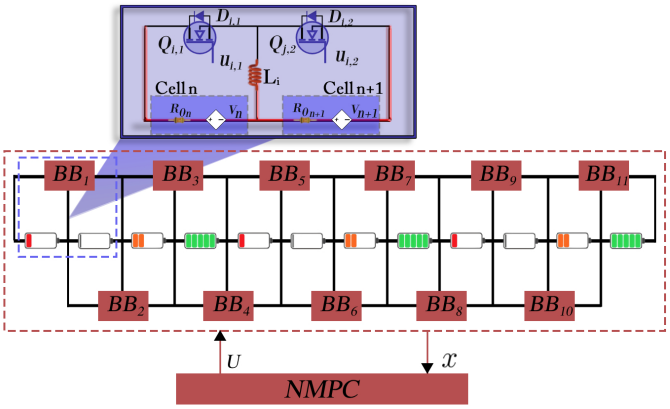


Fig. 1. Schematic of Series-based topology

The dynamics of SoC levels of the cell n and $n+1$ are given as

$$\begin{aligned}\dot{x}_n &= \eta_n^{-1} I_{b_n}(x_n, x_{n+1}, u_{i,1}, u_{i,2}),\\ \dot{x}_{n+1} &= \eta_{n+1}^{-1} I_{b_{n+1}}(x_n, x_{n+1}, u_{i,1}, u_{i,2}),\end{aligned} \tag{1}$$

where x_n, η_n and I_{b_n} represent SoC level, coulombic efficiency and current (A) of the cell n, respectively; and $u_{i,1}$ and $u_{i,2}$ are the control inputs, which are duty cycles of MOSFETs $Q_{i,1}$ and $Q_{i,2}$ of the BB converter i.

Depending on x_n and x_{n+1} the charge transfer between the cells in Fig. 1 is accomplished in the following manner. If $x_n > x_{n+1}$, $Q_{i,1}$ is turned on using $u_{i,1}$, which allows cell n to charge the inductor L_i. Later, when both MOSFETs are open, a discharging current flows from L_i to cell $n+1$ through the body diode $D_{i,2}$, hence accomplishing the charge transfer from cell n to $n+1$. Similarly, when $x_{n+1} > x_n$, $u_{i,2}$ can be employed to transfer charge in the reverse direction. This transfer of charge from high-SoC cell to low-SoC cell continues until the SoC levels of the cells are balanced. The charging and discharging currents of L_i are collectively known as balancing currents, which depend upon various static and dynamic parameters of the network in Fig. 1. The following high-fidelity mean balancing current model is used in this work, which is adapted from our earlier work Javed et al. (2024b).

$$I_{c_{i,j}} = \frac{v_h}{TR_{c_i}}\left(u_{i,j}T - t_d + \tau_{c_i}\left(e^{\kappa_i} - 1\right)\right), \tag{2}$$

$$I_{d_{i,j}} = \frac{\tau_{d_i}\left(e^{\chi_i} - 1\right)}{T}\left(-I_{p_i} - \frac{a_{0_i}(t_{0_i} - u_{i,j}T)}{\tau_{d_i}\left(e^{\chi_i} - 1\right)} + 1\right), \tag{3}$$

$$t_{0_i} = u_{i,j}T + \tau_{d_i} ln\left(\frac{R_{d_i} v_h}{(v_l + V_{F_{i,j}})R_{c_i}}\left(1 - e^{\kappa_i}\right) + 1\right),$$

$$\chi_i = \frac{u_{i,j}T - t_{0_i}}{\tau_{d_i}},\ a_{0_i} = \frac{v_l + V_{F_{i,j}}}{R_{d_i}}.$$

$$I_{p_i} = \frac{v_h}{R_{c_i}}\left(1 - e^{\kappa_i}\right),\ \kappa_i = \frac{t_d - u_{i,j}T}{\tau_{c_i}},$$

$$\lambda_i = \frac{t_d - t}{\tau_{c_i}},\ \phi_{i,j} = \frac{u_{i,j}T - t}{\tau_{d_i}},\ R_{d_i} = R_{0_l} + R_{L_i},$$

$$R_{c_i} = R_{0_h} + R_{L_i} + R_{ds},\ \tau_{c_i} = L_i/R_{c_i},\ \tau_{d_i} = L_i/R_{d_i},$$

where $I_{c_{i,j}}$ and $I_{d_{i,j}}$ represent the charging and discharging currents of BB converter i $(i = 1, 2, \ldots, N-1)$ and its MOSFET j $(j = 1, 2)$; $v_h = \max(v_n, v_{n+1})$ and $v_l = \min(v_n, v_{n+1})$, and R_{0_h} and R_{0_l} are the higher and lower open circuit voltages (V) and series resistances (Ω) of two adjacent higher and lower SoC cells, respectively; $V_{F_{i,j}}$ is the forward voltage drop of diode $D_{i,j}$ parallel to MOSFET $Q_{i,j}$ (cf. Fig. 1); τ_c and τ_d are time constants (s) for charging and discharging of inductor i, respectively; I_{p_i} is the peak inductor current at $t = u_{i,j}T$; t_d, t_{0_i} and T represent dead time, time instant at which inductor current is zero, and switching time period, respectively; duty cycle of $Q_{i,j}$ is denoted by $u_{i,j}$, and L_i represents the inductance of the inductor i (H); R_{L_i}, R_{ds}, R_{c_i} and R_{d_i} represent resistances of inductor, on-state switching, and charging and discharging paths of inductor, respectively; and the open circuit voltages of cell n and $n+1$ are given as

$$v_n = \sum_{s=1}^{8} p_s x_n^{(8-s)},\quad v_{n+1} = \sum_{s=1}^{8} p_s x_{n+1}^{(8-s)}, \tag{4}$$

where $p = [88.56, -320.46, 472.36, -368.96, 166.57, -44.01, 7.18, 2.95]$.

The expression of current I_{b_n} of the cell n given in (1) is dependent on the type of adjacent cell balancing topology. The mathematical models of the balancing topologies

for charge equalization of the battery pack consisting of $N = 12$ series connected cells are given in the following subsections.

2.2 Series-Based Cell-Cell Topology

To balance the SoC levels of N cells, $N-1$ BB converters are required, as shown in the zoomed image of Fig. 1. The current of the cell n depends upon its positioning in the battery pack, for instance, the first $n = 1$ and the last $n = N$ cells can only transfer/receive charge to/from cell 2 and cell $N-1$, respectively. On the other hand, the cell $1 < n < N$ has two adjacent neighbors, therefore, its net current contains balancing currents of two adjacent BB converters. The total currents of first (I_{b_1}), n (I_{b_n}) and last (I_{b_N}) cells are characterized as

$$\begin{aligned}
&I_{b_1}(\boldsymbol{x},\boldsymbol{u}) = -I_{c_{1,1}}(x_1,u_{1,1}) + I_{d_{1,2}}(x_1,x_2,u_{1,2}),\\
&I_{b_n}(\boldsymbol{x},\boldsymbol{u}) = -I_{c_{n,1}}(x_n,u_{n,1}) - I_{c_{(n-1),2}}(x_n,u_{(n-1),2})\\
&+ I_{d_{(n-1),1}}(x_{n-1},x_n,u_{(n-1),1}) + I_{d_{n,2}}(x_n,x_{n+1},u_{n,2})\\
&I_{b_N}(\boldsymbol{x},\boldsymbol{u}) = -I_{c_{(N-1),2}}(x_N,u_{(N-1),2})\\
&+ I_{d_{(N-1),1}}(x_{N-1},x_N,u_{(N-1),1}),
\end{aligned} \tag{5}$$

where $n = 1, 2, \cdots, N$ represents a cell in the battery pack, $\boldsymbol{x} = [x_1\ x_2\ \cdots\ x_N]^T$ is the vector representing SoC levels of the cells, $\boldsymbol{u} = \left[u_{1,1}\ u_{1,2}\ \ldots\ u_{(N-1),1}\ u_{(N-1),2}\right]^T$ is the duty cycle vector.

It is pertinent to mention here that both $I_{c_{i,j}}$ and $I_{d_{i,j}}$ in (2) and (3) are positive; however, a negative sign is assigned to $I_{c_{i,j}}$ in (5). This is due to the current convention followed in this work, according to which a current entering the cell is considered positive, whereas a current going out of a cell is given a negative sign.

2.3 Module-Based Cell-Cell topology

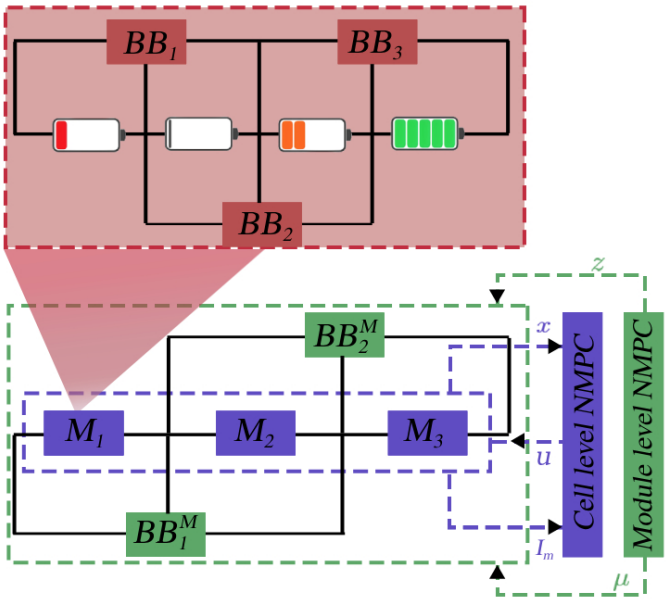


Fig. 2. Schematic of Module-based topology

The total number of cells and the BB converters are similar to the SB cell-cell topology, however, as shown in Fig. 2 the cells are divided into M modules with each module containing N/M cells. The number of BB converters within a module are $N/M - 1$, and there are $M-1$ BB converters to equalize the average SoC of each module. This offers increased balancing speed by equalizing the SoC at the cell and module levels. In this topology the net currents of the cells of the battery pack are given as

$$\begin{aligned}
&I_{b_1} = -I_{c_{1,1}}(\boldsymbol{x},\boldsymbol{u}) + I_{d_{1,2}}(\boldsymbol{x},\boldsymbol{u}) + I_m(\boldsymbol{z},\boldsymbol{\mu}),\\
&I_{b_n} = -I_{c_{n,1}}(\boldsymbol{x},\boldsymbol{u}) - I_{c_{(n-1),2}}(\boldsymbol{x},\boldsymbol{u}) + I_{d_{(n-1),1}}(\boldsymbol{x},\boldsymbol{u})\\
&\quad + I_{d_{n,2}}(\boldsymbol{x},\boldsymbol{u}) + I_m(\boldsymbol{z},\boldsymbol{\mu}),\\
&I_{b_N} = -I_{c_{(N-1),2}}(\boldsymbol{x},\boldsymbol{u}) + I_{d_{(N-1),1}}(\boldsymbol{x},\boldsymbol{u}) + I_m(\boldsymbol{z},\boldsymbol{\mu}),\\
&\boldsymbol{\mu}^T = \left[\mu_{1,1}\ \mu_{1,2}\ \cdots\ \mu_{(M-1),1}\ \mu_{(M-1),2}\right]\\
&\boldsymbol{z}^T = [z_1\ z_2\ \ldots\ z_M]
\end{aligned} \tag{6}$$

where I_m represents the current of module $m \in [1, M]$, which is given by (7); z_m is the average SoC of the cells contained in the module m; and μ is the duty cycle (control input) vector for module level BB converters.

$$\begin{aligned}
&I_1 = -I_{c_{1,1}}(z_1,\mu_{1,1}) + I_{d_{1,2}}(z_1,z_2,\mu_{1,2}),\\
&I_m = -I_{c_{m,1}}(z_m,\mu_{m,1}) - I_{c_{(m-1),2}}(z_m,\mu_{(m-1),2})\\
&+ I_{d_{(m-1),1}}(z_{m-1},z_m,\mu_{(m-1),1}) + I_{d_{m,2}}(z_m,z_{m+1},\mu_{m,2}),\\
&I_M = -I_{c_{(M-1),2}}(z_M,\mu_{(M-1),2})\\
&+ I_{d_{(M-1),1}}(z_{M-1},z_M,\mu_{(M-1),1}).
\end{aligned} \tag{7}$$

2.4 Layer-Based Cell-Cell Topology

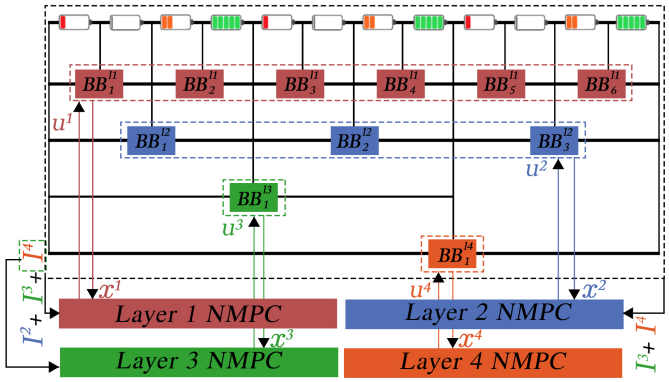


Fig. 3. Schematic of Layer-based topology

In this topology, SoC levels of N cells are equalized by employing $\lceil \log_2^N \rceil$ layers of BB converters, with each layer containing $\lfloor N/2^l \rfloor$ equalizers, where $1 \le l \le L-1$ and L represents the total layers in the topology. It is important to note that the last layer has only one BB converter. The net current of the cell n is given as

$$I_{b_n} = \sum_{l=1}^{L}\left(\sum_{n_l=1}^{2\times\lfloor N/2^l\rfloor} I_{n_l}^l(\boldsymbol{x}^l,\boldsymbol{u}^l)\right) + I_{n_L}^L(\boldsymbol{x}^L,\boldsymbol{u}^L) \tag{8}$$

$$I_{n_l}^l = \begin{cases} -I_{c_{r_l,1}}(u_{r_l,1}^l, x_{n_l}^l) + I_{d_{r_l,2}}(u_{r_l,2}^l, x_{n_l}^l, x_{n_l+1}^l) \\ -I_{c_{r_l,2}}(u_{r_l,2}^l, x_{n_l}^l) + I_{d_{r_l,1}}(u_{r_l,1}^l, x_{n_l-1}^l, x_{n_l}^l) \end{cases},$$

$$I_{n_L}^L = \begin{cases} -I_{c_{1,1}}(u_{1,1}^L, x_1^L) + I_{d_{1,2}}(u_{1,2}^L, x_1^L, x_2^L) & 1^{\text{st}}\text{ cell} \\ -I_{c_{1,2}}(u_{1,2}^L, x_2^L) + I_{d_{1,1}}(u_{1,1}^L, x_1^L, x_2^L) & 2^{\text{nd}}\text{ cell} \end{cases},$$

where, n_l is odd, n_l is even and $I_{n_l}^l$ is the current of cell n_l in layer l; the duty cycle vector of layer l is given is $\boldsymbol{u}^l = \{u_{r_l}^l\}$, where $r_l = 1, 2, \ldots, \lfloor N/2^l \rfloor$; $\boldsymbol{x}^l = \{x_{n_l}^l\}$ with

$n_l = 1, 2, \ldots, 2 \times \lfloor N/2^l \rfloor$ represents the SoC vector of layer l; and $u^L = \begin{bmatrix} u_1^L & u_2^L \end{bmatrix}^T$ and $x^L = \begin{bmatrix} x_1^L & x_2^L \end{bmatrix}^T$ are duty cycle and SoC vectors of the last layer.

As shown in Fig. 3 there is a dedicated BB converter for each pair of cells in $l = 1$. Whereas, for $l > 1$, each equalizer balances the average SoC levels of cells on its left and right sides. The expression for net current of cell n in (8) might look ambiguous initially; however, from Fig. 3 it can be seen that the current of each layer contributes in I_{b_n}

3. NONLINEAR MODEL PREDICTIVE CONTROL DESIGN FOR CELL-CELL TOPOLOGIES

Due to the nonlinearity in the expressions of charging and discharging currents in (2) and (3), the SoC dynamics of cell n (1) are nonlinear; therefore, in the subsequent subsections, the NMPC problem is formulated for balancing the SoC level of cells for the aforementioned topologies.

3.1 NMPC Design for Series-Based Cell-Cell Topology

Only one NMPC is required to equalize the SoC levels of the cells in this topology. The optimal control problem in this case is given as

$$\min_{\boldsymbol{x(k)},\boldsymbol{\nu(k)}} J(\boldsymbol{x(k)}, \boldsymbol{\nu(k)}), \tag{9}$$

$$J = \sum_{k=k_0}^{k_0+H_p} \sum_{n=1}^{N} \Big(x_n(k) - \bar{x}(k) \Big)^2,$$

$$\bar{x}(k) = \frac{1}{N} \sum_{n=1}^{N} x_n(k),$$

subject to

$$\boldsymbol{x(k+1)} - \tilde{\boldsymbol{f}}(\boldsymbol{x(k)}, \boldsymbol{\nu(k)}) = 0, \tag{9a}$$
$$\boldsymbol{x}(k_0) = \boldsymbol{x}_{k_0}, \tag{9b}$$
$$\nu_{i,k} \in [0,\ 0.4 - t_d/T], \tag{9c}$$
$$x_n(k) \in [0.05,\ 0.95], \tag{9d}$$
$$\boldsymbol{\nu}_{i,1}^T(k) \boldsymbol{\nu}_{i,2}(k) = 0, \tag{9e}$$

where $\boldsymbol{x}^T(k) = [x_1(k)\ x_2(k)\ \ldots\ x_N(k)]$ is the vector representing SoC levels of cells; $\boldsymbol{\nu}(k) = \boldsymbol{u}(k) - t_d/T$; $\tilde{\boldsymbol{f}}$ is the discrete version of $\boldsymbol{f}^T = \begin{bmatrix} \eta_1^{-1} I_{b_1} & \eta_2^{-1} I_{b_2} & \ldots \eta_N^{-1} I_{b_N} \end{bmatrix}$; $\boldsymbol{x}_{k_0}$ is the vector of current cell's SoC at k_0; $\boldsymbol{\nu}_{i,1}^T(k) = [\nu_{1,1}\ \nu_{2,1} \ldots\ \nu_{N-1,1}]$ and $\boldsymbol{\nu}_{i,2}^T(k) = [\nu_{1,2}\ \nu_{2,2} \ldots\ \nu_{N-1,2}]$. The constraint in (9e) is added so that both MOSFETs of a BB converter do not turn on simultaneously.

3.2 NMPC Design for Module-Based Cell-Cell Topology

As shown in Fig. 2 there are two levels of NMPC: module-level NMPC, which balances the SoC levels of the module, and cell-level NMPC, which equalizes the cell's SoC levels. The NMPC formulation for both the controllers is given below

$$\min_{\boldsymbol{z(k)},\boldsymbol{w(k)}} J(\boldsymbol{z(k)}, \boldsymbol{w(k)}), \tag{10}$$

$$J = \sum_{k=k_0}^{k_0+H_p} \sum_{m=1}^{M} \Big(z_m(k) - \bar{z}(k) \Big)^2,$$

$$\bar{z}(k) = \frac{1}{M} \sum_{m=1}^{N} z_m(k),$$

subject to

$$\boldsymbol{z(k+1)} - \tilde{\boldsymbol{g}}(\boldsymbol{z(k)}, \boldsymbol{w(k)}) = 0, \tag{10a}$$
$$\boldsymbol{z}(k_0) = \boldsymbol{z}_{k_0}, \tag{10b}$$
$$w_{i,k} \in [0,\ 0.4 - t_d/T], \tag{10c}$$
$$z_n(k) \in [0.05,\ 0.95], \tag{10d}$$
$$\boldsymbol{w}_{i,1}^T(k) \boldsymbol{w}_{i,2}(k) = 0, \tag{10e}$$

where $\boldsymbol{z}^T(k) = [z_1(k)\ z_2(k)\ \ldots\ z_M(k)]$ is the vector representing SoC levels of cells; $\boldsymbol{w}(k) = \boldsymbol{\mu}(k) - t_d/T$; $\tilde{\boldsymbol{g}}$ is the discrete version of $\boldsymbol{g}^T = \begin{bmatrix} \eta_1^{-1} I_1 & \eta_2^{-1} I_2 & \ldots \eta_M^{-1} I_M \end{bmatrix}$; $\boldsymbol{z}_{k_0}$ is the vector of module SoC at k_0; $\boldsymbol{w}_{i,1}$ and $\boldsymbol{w}_{i,2}$ are modified control input vectors for the first and second MOSFETs of the module level BB converters.

The cell level NMPC problem formulation in MB cell-cell topology is similar to (9) but the dynamics of the cell represented by f is different-

$$\boldsymbol{f}^T = \begin{bmatrix} \eta_1^{-1} I_{b_1} + I_m & \eta_2^{-1} I_{b_2} + I_m & \ldots \\ \eta_N^{-1} I_{b_N} + I_m \end{bmatrix},$$

where I_m is the current of the module that contains the cell.

3.3 NMPC Design for Layer-Based Cell-Cell Topology

From Fig. 3 it is evident that there is separate NMPC for each layer. A generalized NMPC formulation for layer l is given as

$$\min_{\boldsymbol{x}^l(k),\boldsymbol{\mathcal{U}}^l(k)} J^l(\boldsymbol{x}^l(k), \boldsymbol{\mathcal{U}}^l(k)), \tag{11}$$

$$J^l = \sum_{k=k_0}^{k_0+H_p} \Bigg[\sum_{n_l=1}^{2\times\lfloor N/2^l \rfloor} \Big(x_{n_l}^l(k) - \bar{x}^l(k) \Big)^2 + \sum_{n_L=1}^{2} \Big(x_{n_L}^L(k) - \bar{x}^L(k) \Big)^2 \Bigg]$$

$$\bar{x}^l(k) = \frac{1}{M} \sum_{n_l=1}^{2\times\lfloor N/2^l \rfloor} x_{n_l}^l(k), \quad \bar{x}^L(k) = \frac{1}{2} \sum_{n_L=1}^{2} x_{n_L}^L(k),$$

subject to

$$\boldsymbol{x}^l(k+1) - \tilde{\boldsymbol{h}}^{\boldsymbol{l}}(\boldsymbol{x}^{\boldsymbol{l}}(\boldsymbol{k}), \boldsymbol{\mathcal{U}}^{\boldsymbol{l}}(\boldsymbol{k})) = 0, \tag{11a}$$
$$\boldsymbol{x}^l(k_0) = \boldsymbol{x}_{k_0}^l, \tag{11b}$$
$$\mathcal{U}_{n_l,k}^l \in [0,\ 0.4 - t_d/T], \tag{11c}$$
$$x_{n_l}^l(k) \in [0.05,\ 0.95], \tag{11d}$$
$$\boldsymbol{\mathcal{U}}^{l^T}_{n_l,1}(k) \boldsymbol{\mathcal{U}}_{n_l,2}^l(k) = 0, \tag{11e}$$

where $\boldsymbol{x}^l$ is the SoC level of cell n for $l = 1$, and for $l > 1$ it represents the average SoC dynamics of the cells on the left and right side of the BB converters (see Fig. 3) in layer l; $\boldsymbol{\mathcal{U}}^l = \boldsymbol{u}^l - t_d/T$; and $\tilde{\boldsymbol{h}}^l$ is the discrete version of $\boldsymbol{h}^l$, which is given as

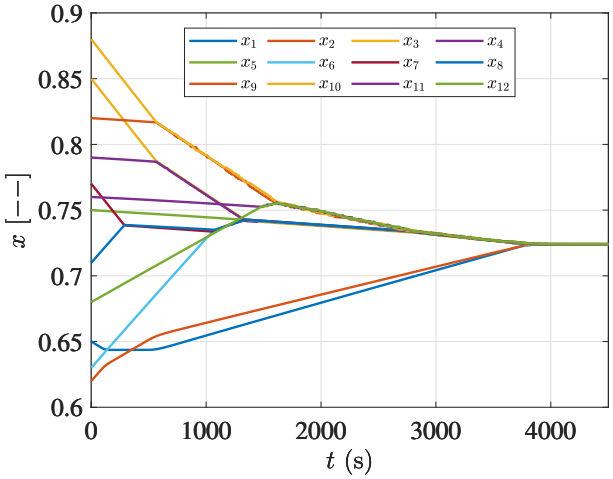


Fig. 4. State of charge for series-based cell-cell topology.

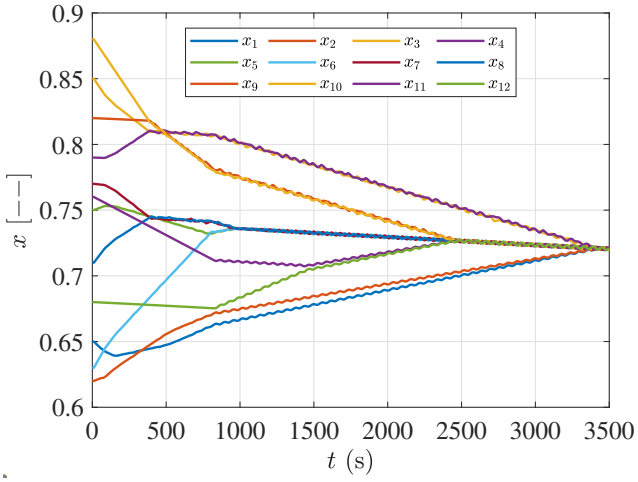


Fig. 5. State of charge for module-based cell-cell topology.

$$\boldsymbol{h}^{l^T} = \left[\eta_1^{-1}\sum_{l}^{L} I_1^l \;\; \eta_2^{-1}\sum_{l}^{L} I_2^l \;\; \ldots \;\; \eta_{n_l}^{-1}\sum_{l}^{L} I_{n_l}^l\right] \tag{12}$$

4. RESULTS AND DISCUSSIONS

The aim of this work was to evaluate the performance, i.e., BT, of three different topologies using the high-fidelity balancing current within the NMPC framework. We have performed simulations on twelve serially connected cells, the parameters of which are adopted from Uppal et al. (2023). Moreover, the balancing criterion is when the standard deviation of cells' SoC $\sigma(\boldsymbol{x})$ becomes equal to 0.01. Figures 4, 5, and 6 depict the evolution of SoC for SB, MB, and LB topologies, respectively. These figures show that for a specific $\boldsymbol{x_0}$, all the topologies have been able to equalize the pack. However, their respective BTs vary, as illustrated in Figure 7; for instance, the BTs are 2980, 2770, and 1430 s for SB, MB, and LB topology, respectively. Apart from achieving the fastest balancing, LB topology is also computationally feasible, with a computational time of 360 s; whereas MB and SB took 1800 and 2700 s, respectively, on a Core(TM) i7 CPU @ 1.80 GHz and 16.0 GB of RAM. This is because, for LB topology, the NMPC problem becomes sparse due to a dedicated BB converter for each pair of cells in each layer. Moreover, Figures 8, 9, and 10 show the 22 duty cycles—with 2 for each BB converter—for SB, MB, and LB topologies, respectively.

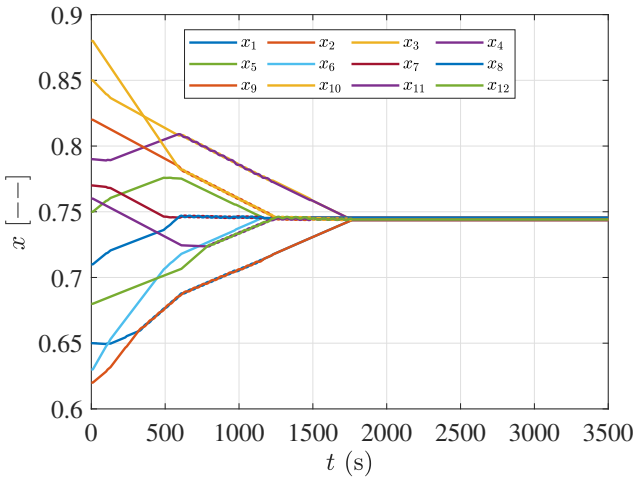
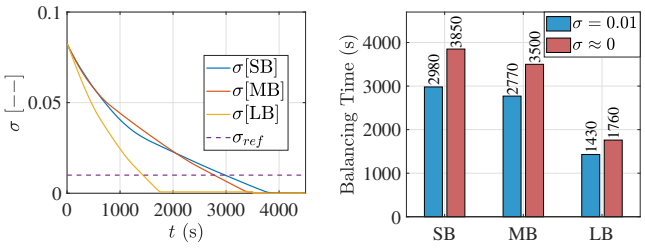


Fig. 6. State of charge for layer-based cell-cell topology.



(a) Standard deviation (b) Balancing time

Fig. 7. Comparison of the standard deviation of SoCs and balancing time for each topology.

5. CONCLUSION

The future work aims to extend this work by including non-adjacent-based topologies as well as quantifying their impacts at the system level, i.e., range extension of EVs.

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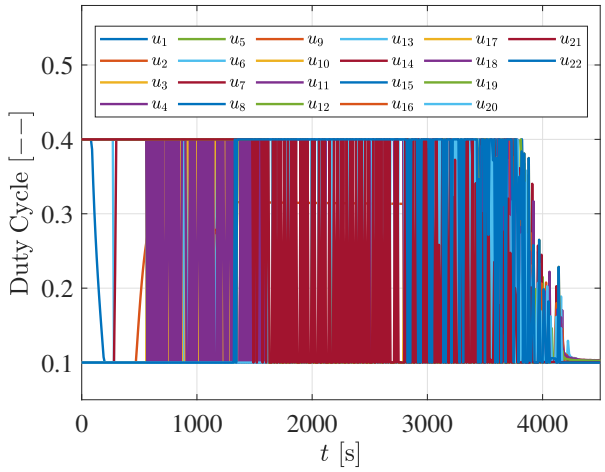

Fig. 8. Control input/duty cycle for series topology.

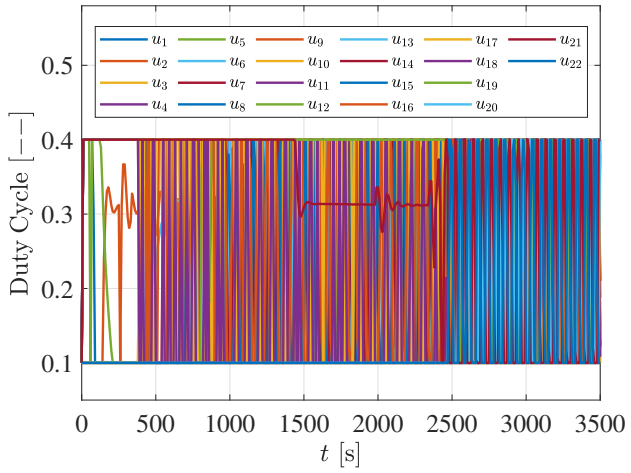

Fig. 9. Control input/duty cycle for module-based topology.

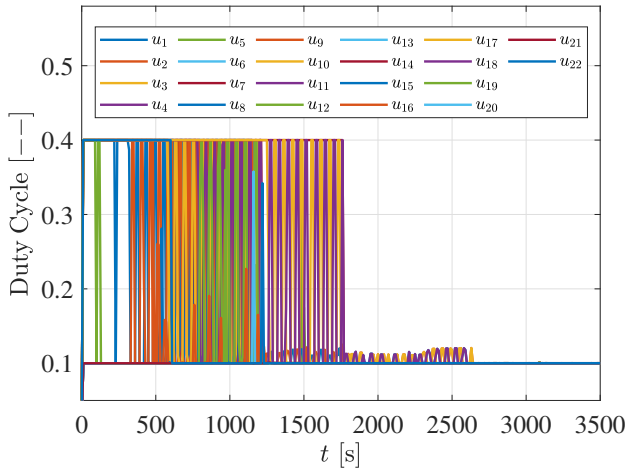

Fig. 10. Control input/duty cycle for layer-based topology.

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